From chip level to 12” wafer level 3D processing
Tohoku-MicroTec Co., Ltd.

We provide cutting-edge 3D-IC R&D Prototyping and Pilot / Low-Volume Production Service

- **State-of-the-art technologies**
  - 200mm and 300mm 3D process engineering lines and advanced technology platforms
    - design / layout / mask making
    - wafer / chip thinning
    - forming TSV on chip / wafer (front side / backside TSV)
    - redistribution routing
    - both side u-bumps formation on chip / wafer
    - chip / wafer stacking

- **3D stacking LSIs prototype manufacturing service**
  - Prototyping of proof of concepts using commercial/customized 2D chips
  - die-level 3D hetero-integration with backside TSV technology

- **Support your small-volume, special customized 3D productions**
  - base-line process set-up for the pilot production
  - facilitate your product development

- **2.5D interposer R&D foundry and pilot production service**
  - Large area interposer
  - Interposer with passive devices

- **Development innovative 3D stacking technologies for creative 3D products and applications**

- **Supply IP and special customized TEG wafers for process-induced reliability characterization**

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**Advantages of 3D IC**

**Conventional SoC**
- Compound semiconductor
- Sync. clock
- Long Global interconnect → large RC delay, large $C_p$

**3D-SoC**
- Segment 2D-SoC into functional block
- Short global interconnect
  - small RC delay, small $C_p$
  - High band width
  - Small form factor

- **1. Maximization of electrical performances**
- **2. Increase of circuit density**
- **3. New Architecture (Hyper-parallel processing, Multifunction, etc)**
- **4. Heterogeneous integration**
- **5. Cost reduction**
- **6. Realization of high performance detector with ~100% area factor in chip**

SoC: System on Chip (System LSI)
**Technology / Samples**

**Low cost 3D-Soc Manufacturing Technology**

- TSV Micro-bump
- Heterogeneous Integration
- Low cost fabrication

- Overall view
- 38 chips stack

**TSV Process**

- 0.7μm
- 3μm
- 5-10μm

- Cu TSV (Via middle)
- Cu TSV (Via last)

**2.5D Interposer**

- 12-inch Wafer
- 50mm

**3D-MEMS/Hetero-Integration**

- Vertically Stacked MEMS on LSI Chip
- Hetero-Integrated LSI-MEMS Multi-Chip Module

**MicroProbes for Neural recording**

- Diagnosis and treatment for brain disorder (Double-sided Si Probe)
- Research for BMI/BCI

**Lineup of Neural Microprobes**

- Diagnosis of Epilepsy patient
- Tungsten core Omnidirectional probe

**Others**

- 4-shrink Double-sided Si Probes
- w/ optical waveguide
- w/ fluidic channel
200mm/300mm 3D Integration Process Facilities

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