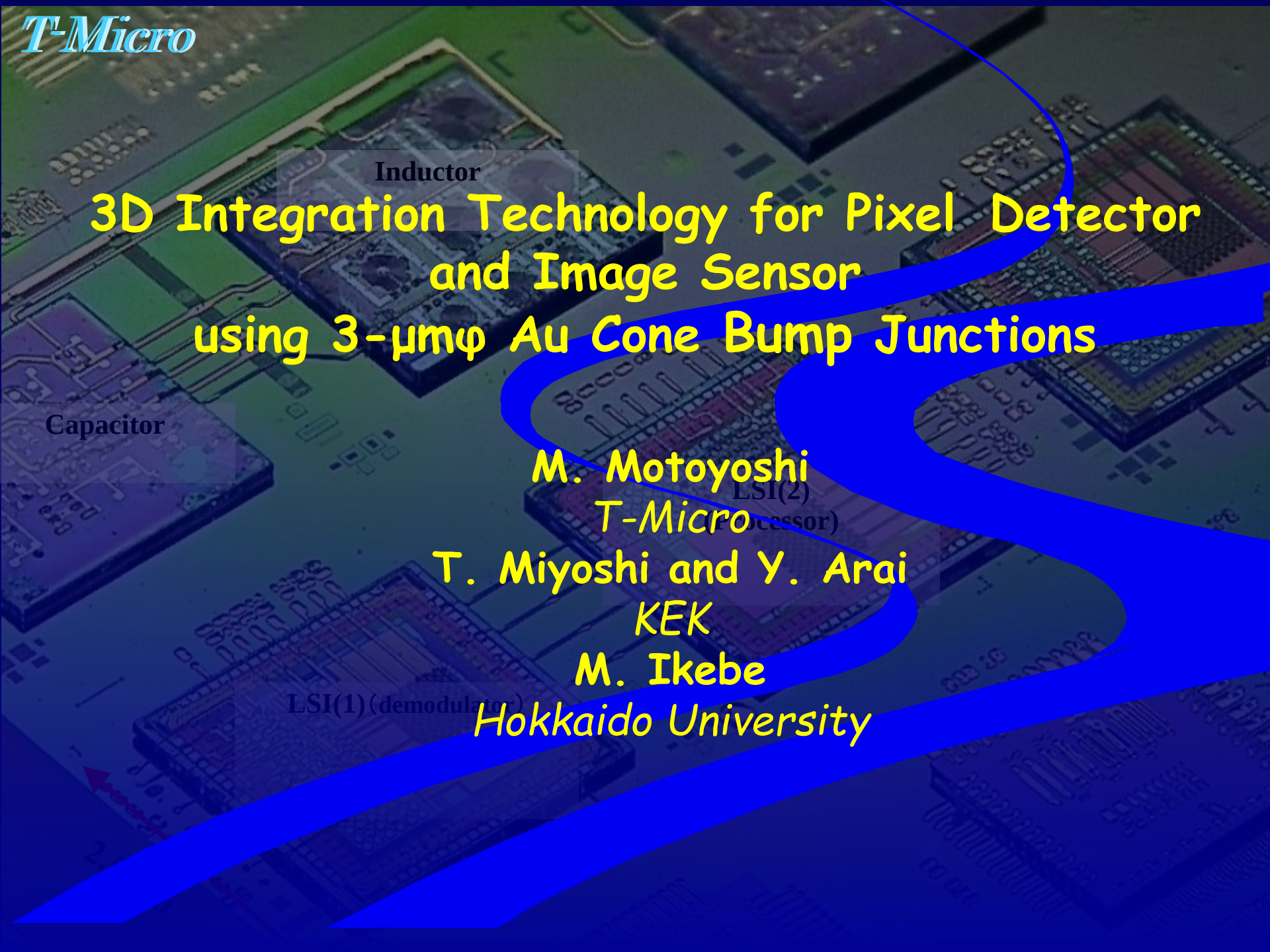


3D Integration Technology for Pixel Detector and Image Sensor using 3-μmφ Au Cone Bump Junctions

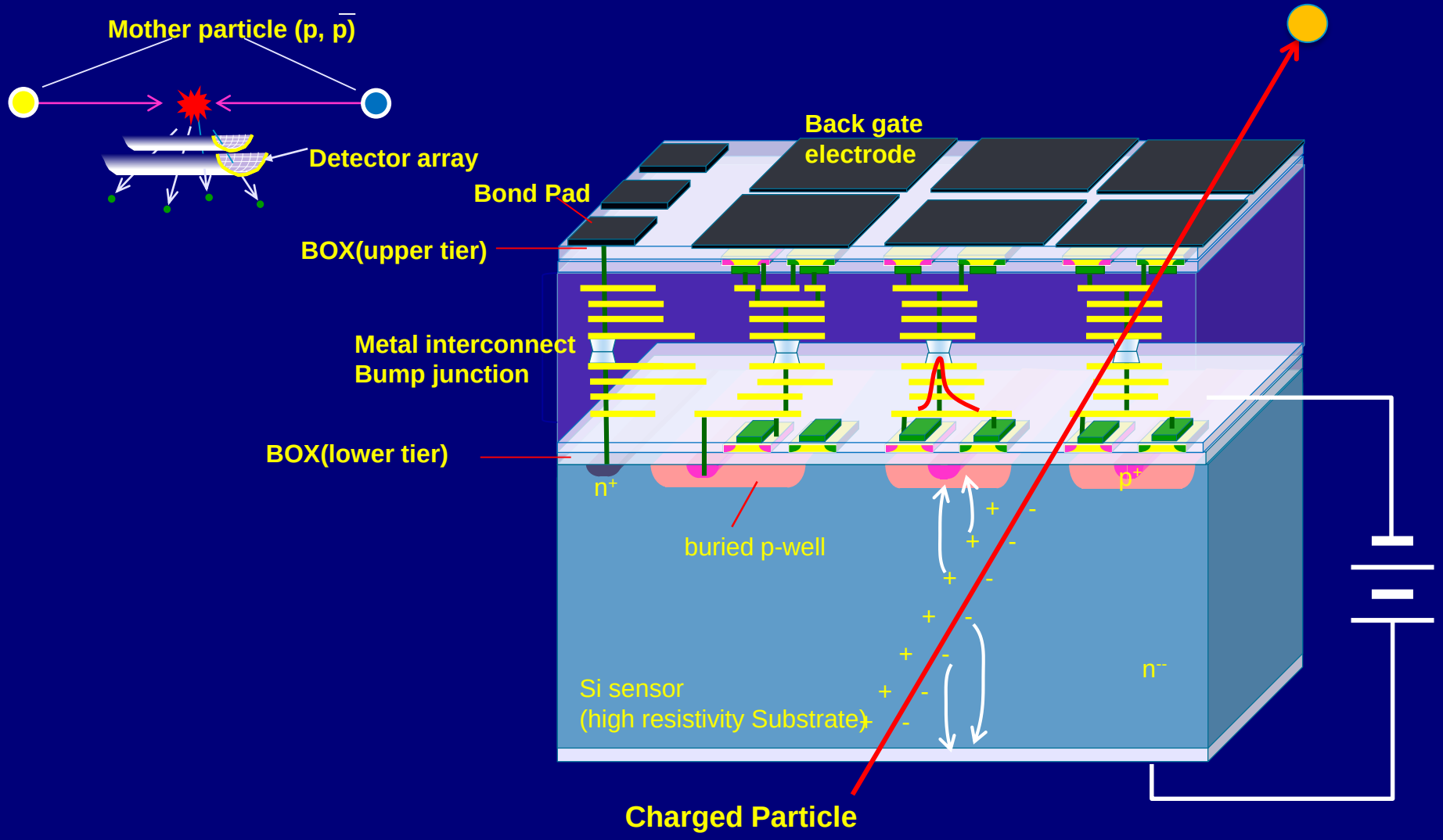
M. Motoyoshi
T-Micro
T. Miyoshi and Y. Arai
KEK
M. Ikebe
Hokkaido University

Contents

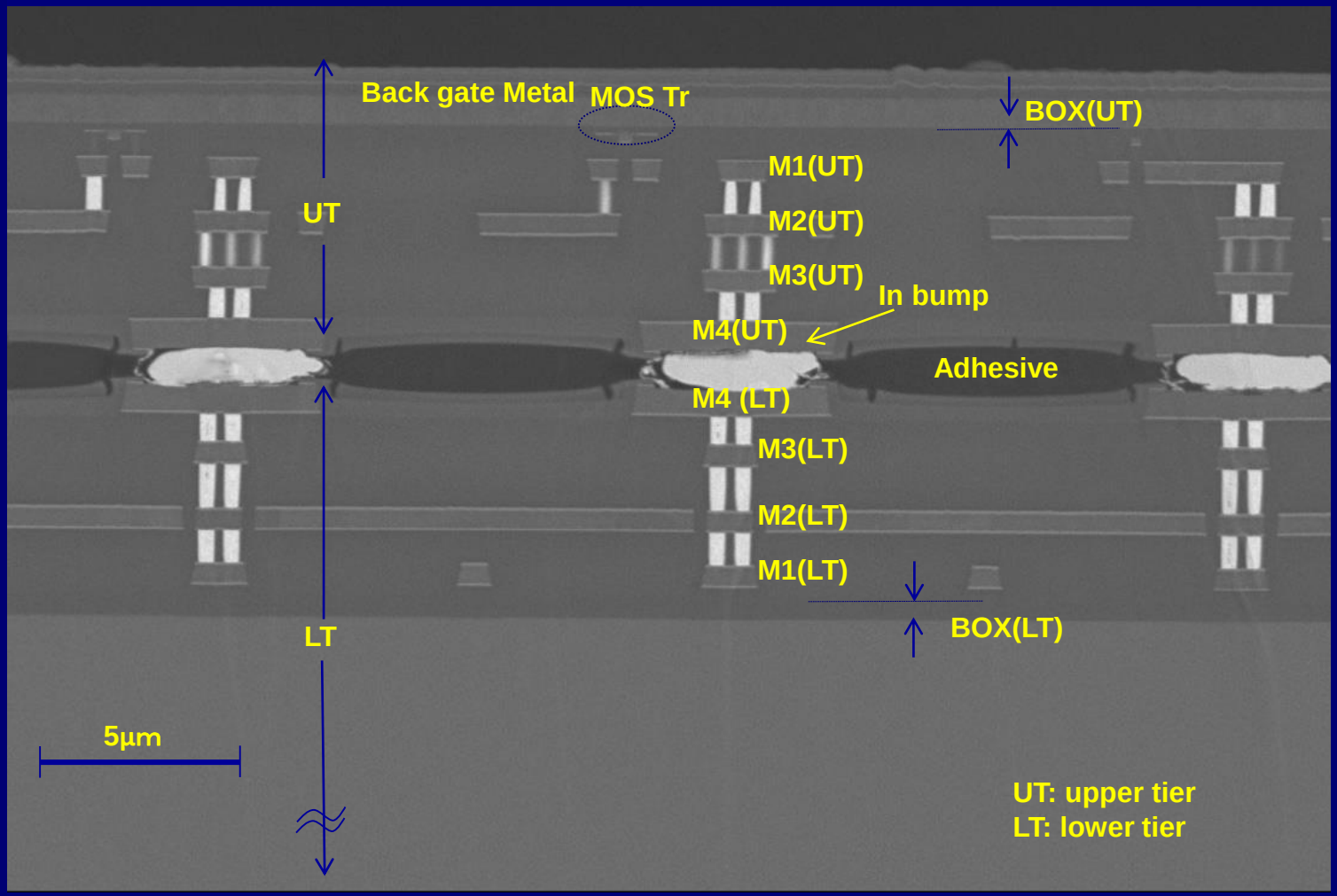
1. Background
   -previous work
2. Au cone bump using NpD
3. 3D Cost reduction approach
4. Summary

NpD: Nano-particle deposition

Stacked SOI Pixel detector

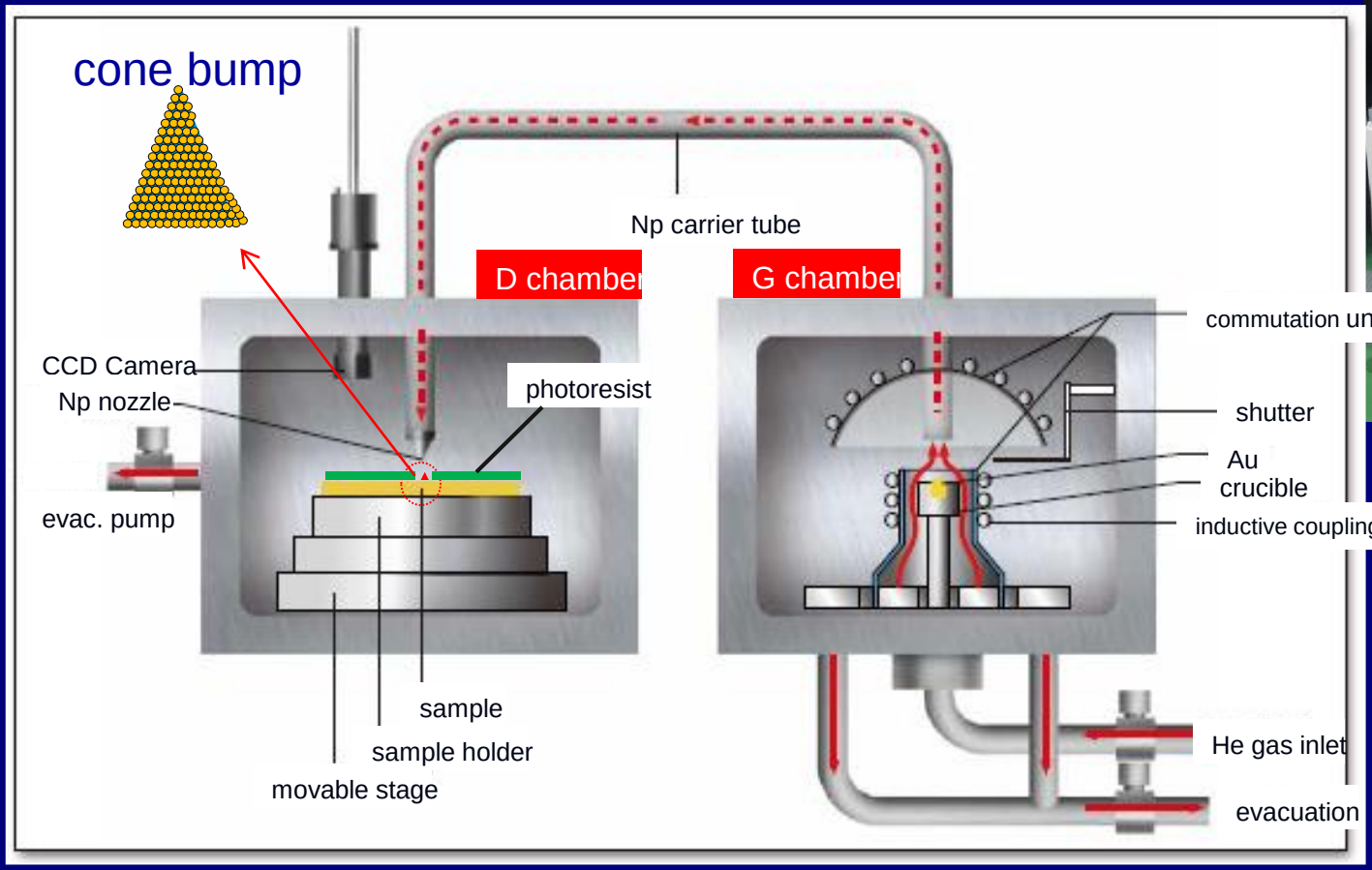


Cross sectional SEM image of pixel array using Indium micro-bump



2. Au cone bump using NpD

Nano-particle Deposition (NpD) System



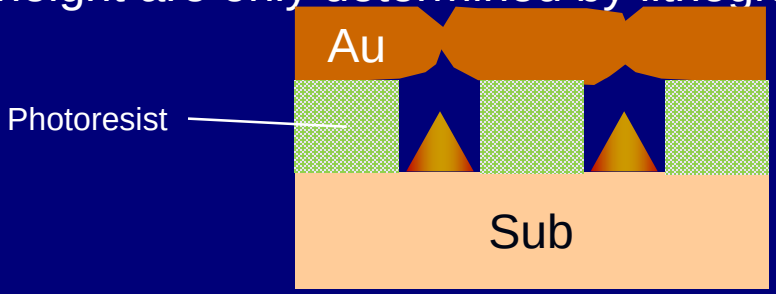
Courtesy of MIKUNI KOGYO Co., Ltd

Pros & cons of Au cone bump

Pros

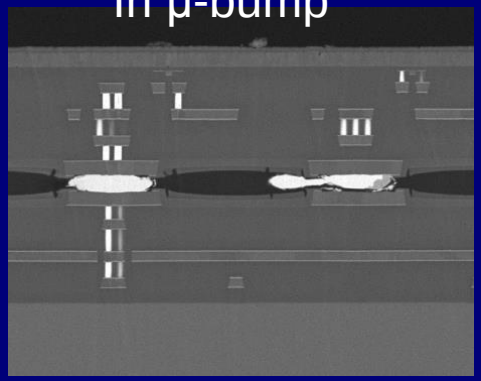
- good scalability

-bump size and height are only determined by lithography process

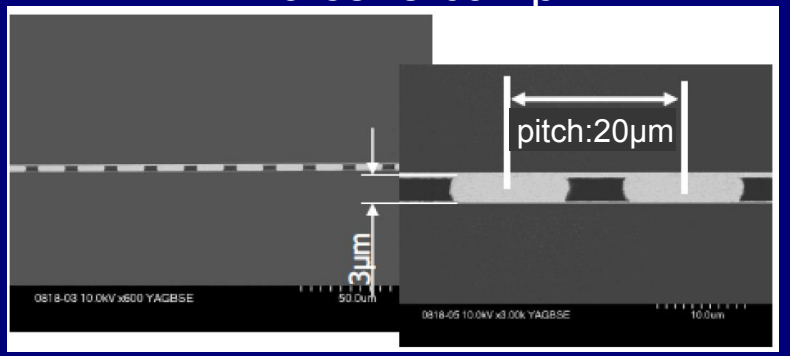


-no extrusion

In μ-bump



Au cone bump



Pros & cons of Au cone bump

Pros

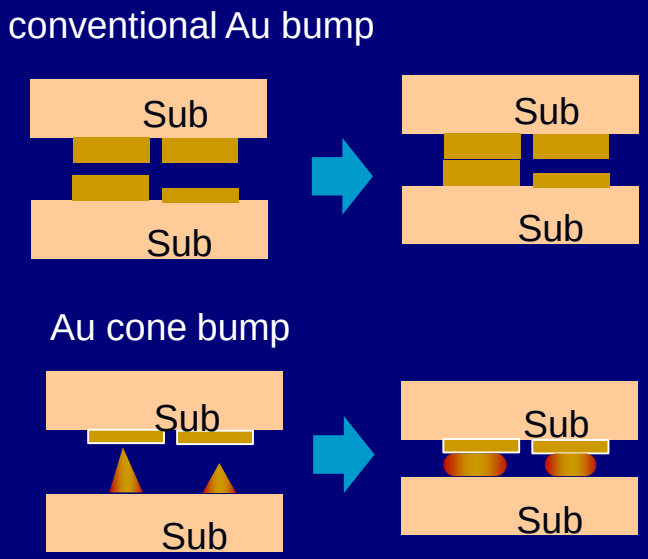
- good scalability

  -bump size and height are only determined by lithography process

  -no extrusion

- large bonding margin

  NpD Au cone bump➔easy to deform
  Au ➔ → oxidation resistant material



Pros & cons of Au cone bump

Pros

- good scalability
  - -bump size and height are only determined by lithography process
  - -no extrusion
- large bonding margin

NpD Au cone bump➔easy to deform
Au ➔ → oxidation resistant material

- low temperature process

less than 200 ℃ ➔ 120℃(our target)

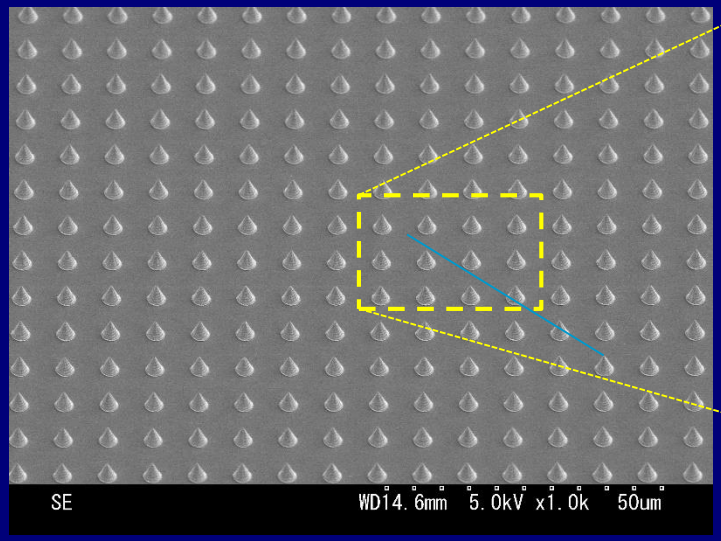
Cons

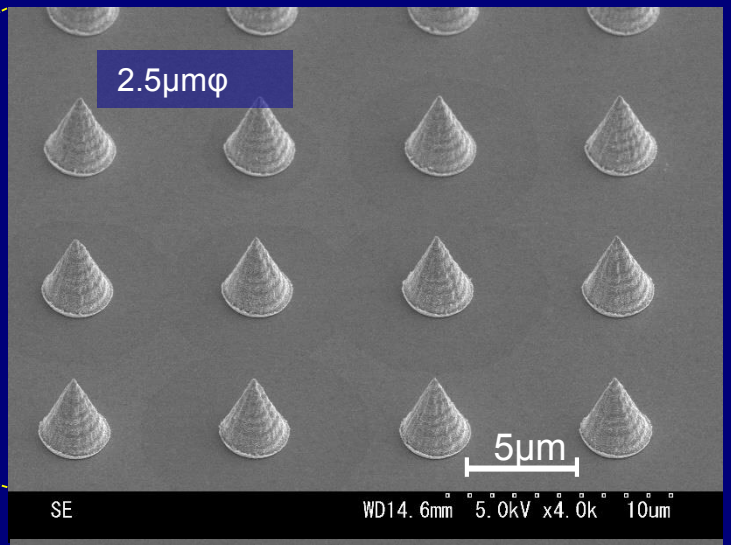
- low throughput

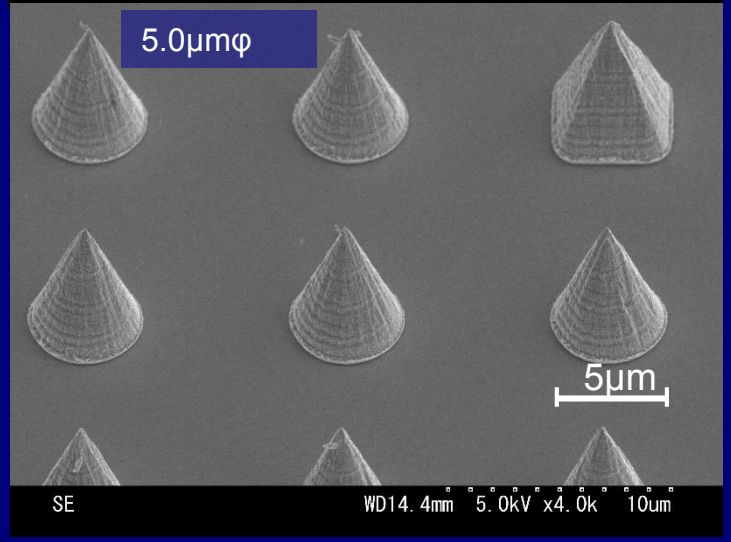
Current process time for 5mm x 5mm chip is around 1hour

⟶ An improvement of deposition speed is now in progress

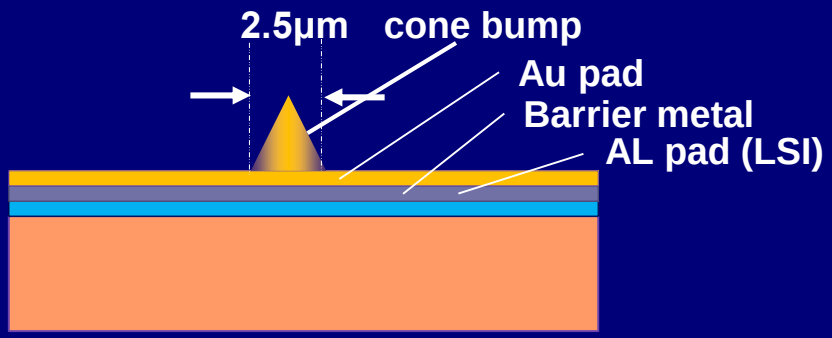
2.5/5.0μmφ Au Cone Bump







TEG cross section



Process flow for SOI Pixel detector(1)

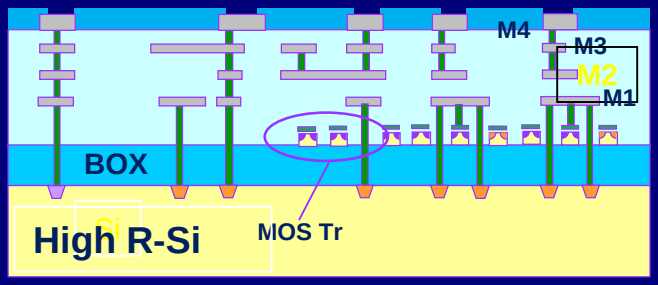
< Lower Tier >

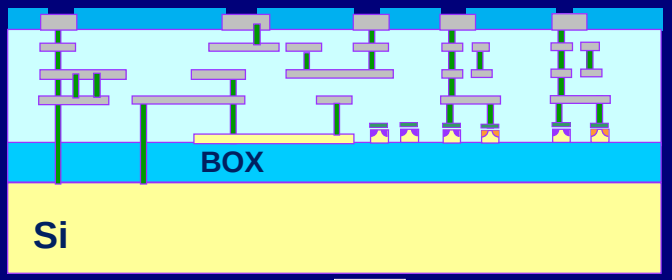
< Upper Tier >

(a) Start with FD-SOI device wafer

Active Si~50 nm
BOX:200 nm

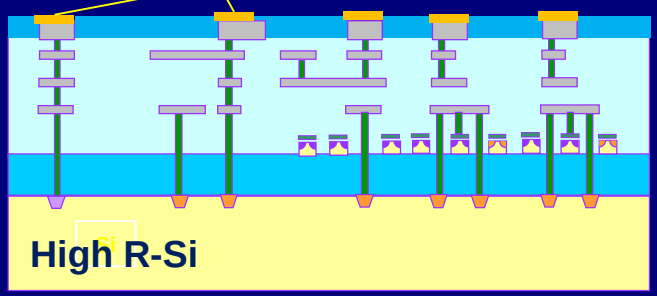
**FD: Fully Depleted*



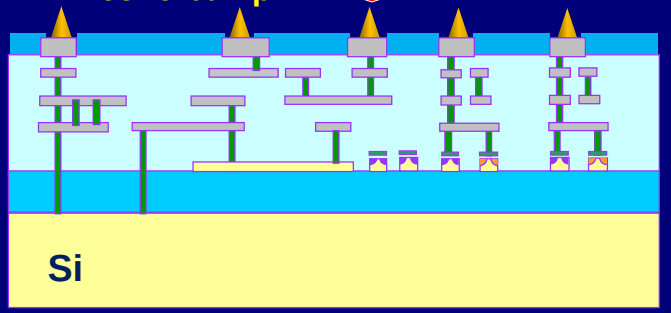


bump-landing pad

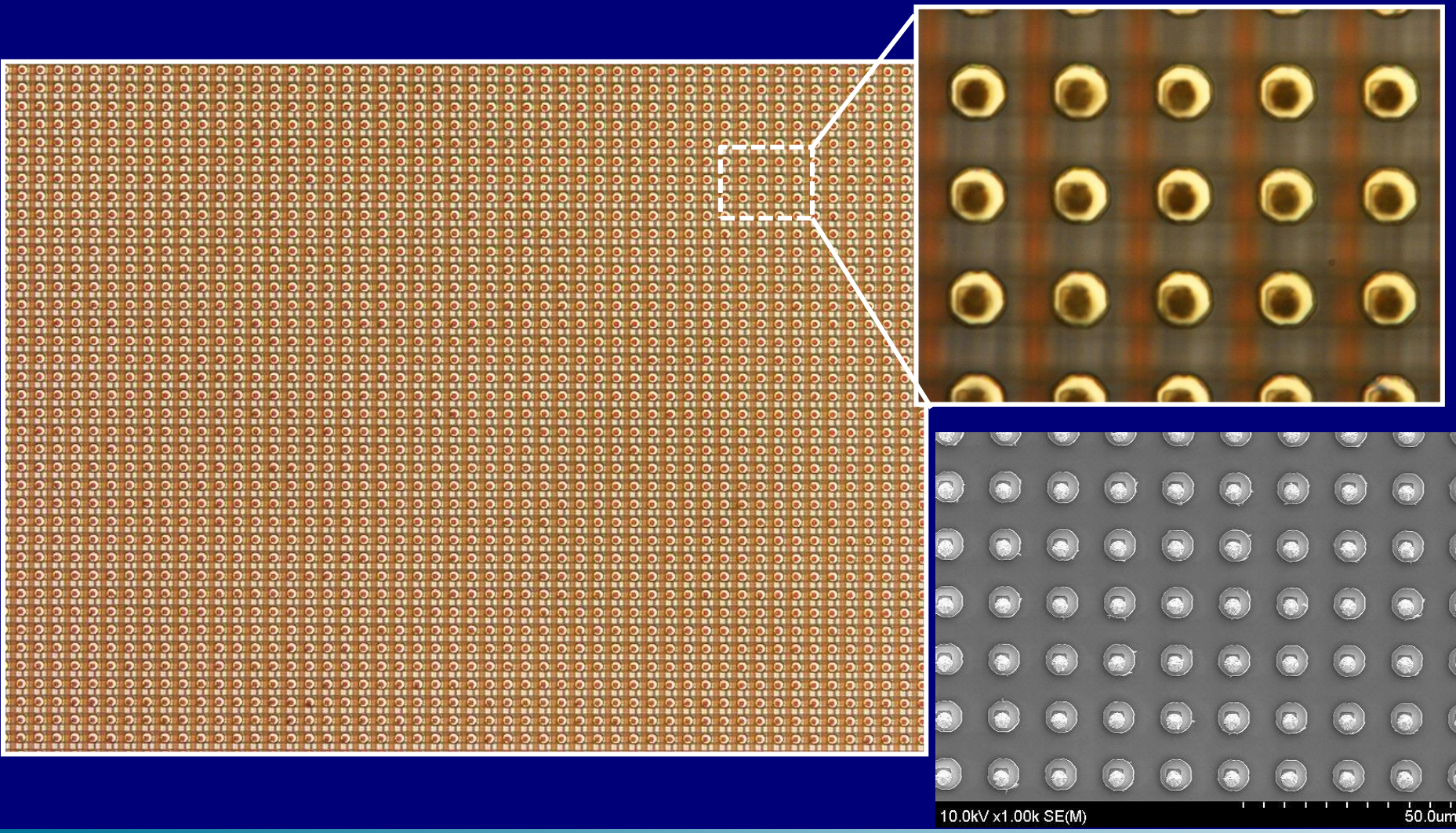
(b) cone bump/ landing-pad forming



cone-bump



After cone bump formation (@ pixel array area)



Process flow for SOI Pixel detector(1)

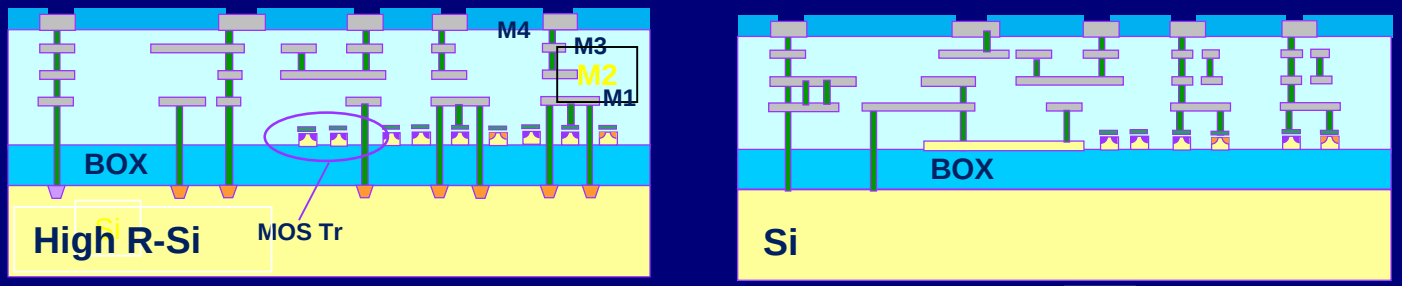
< Lower Tier >

< Upper Tier >

(a) Start with FD-SOI device wafer

Active Si~50 nm
BOX:200 nm

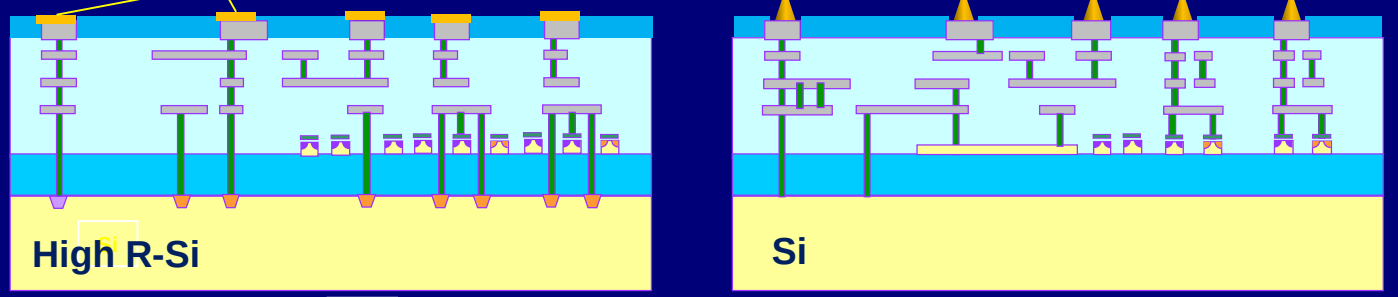
**FD: Fully Depleted*



bump-landing pad

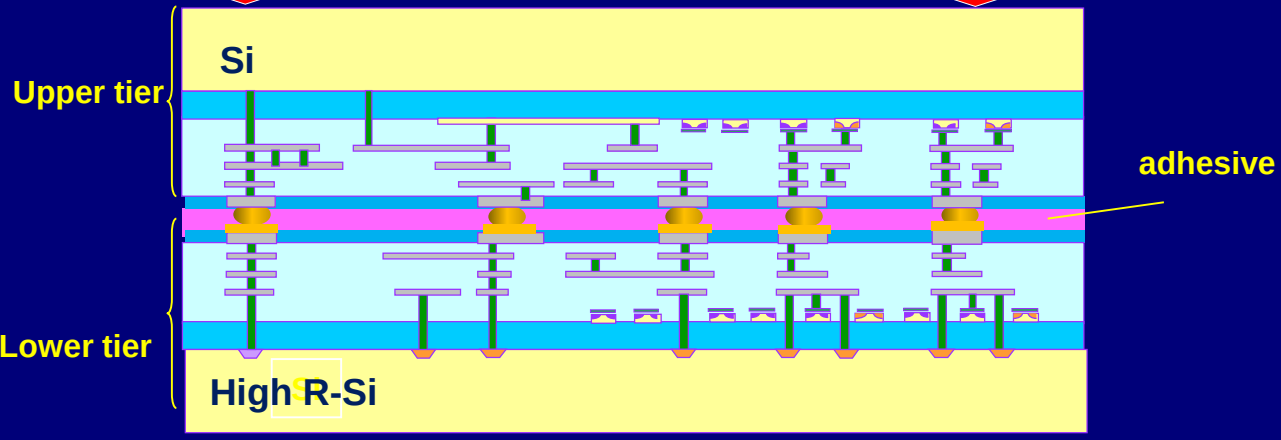
cone-bump

(b) cone bump/ landing-pad forming



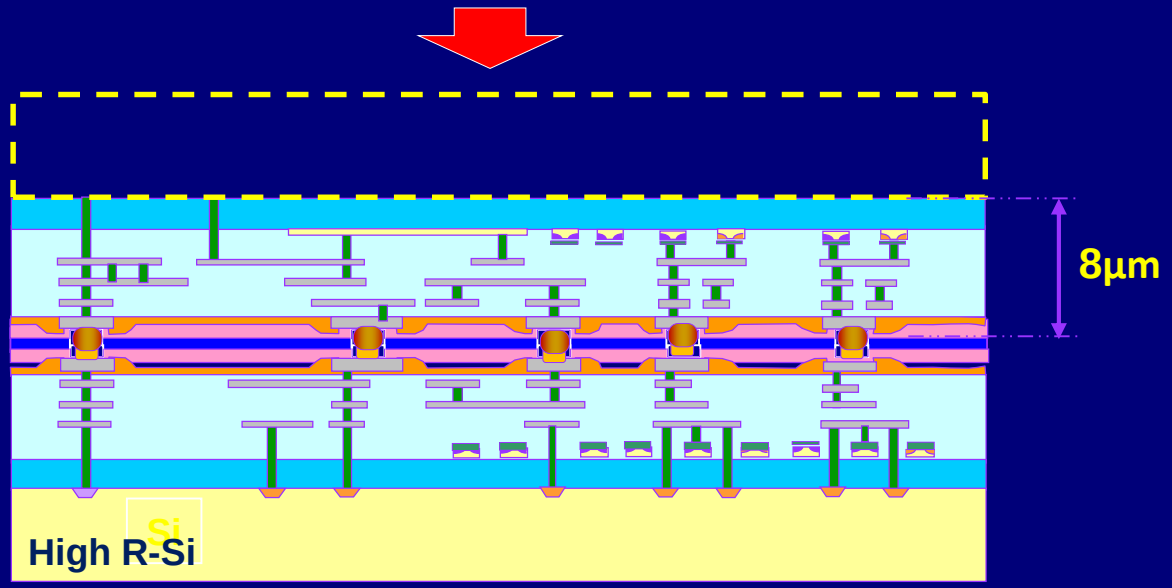
(c) Chip bonding

- face to face infrared alignment
- bonding (<200℃)
-Adhesive injection

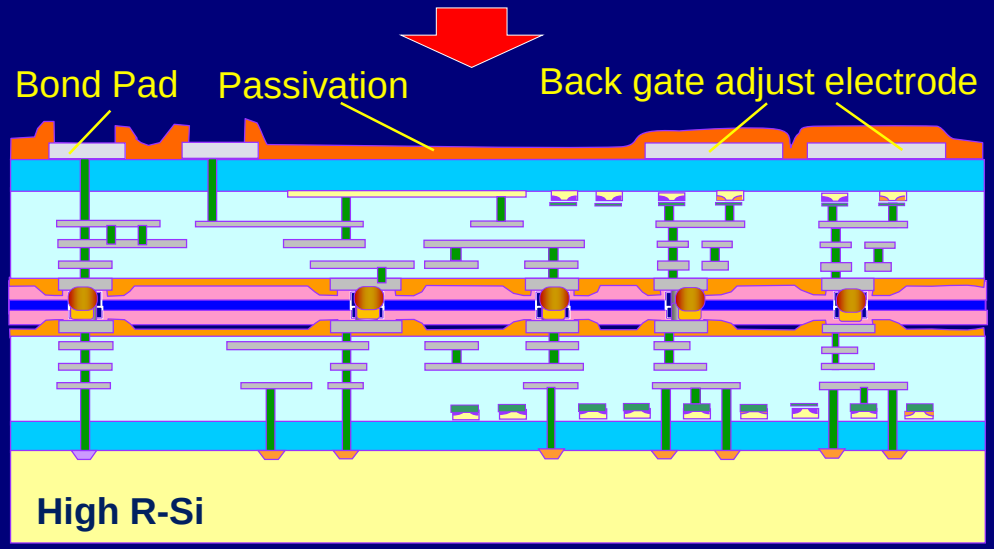


Process flow for SOI Pixel detector(2)

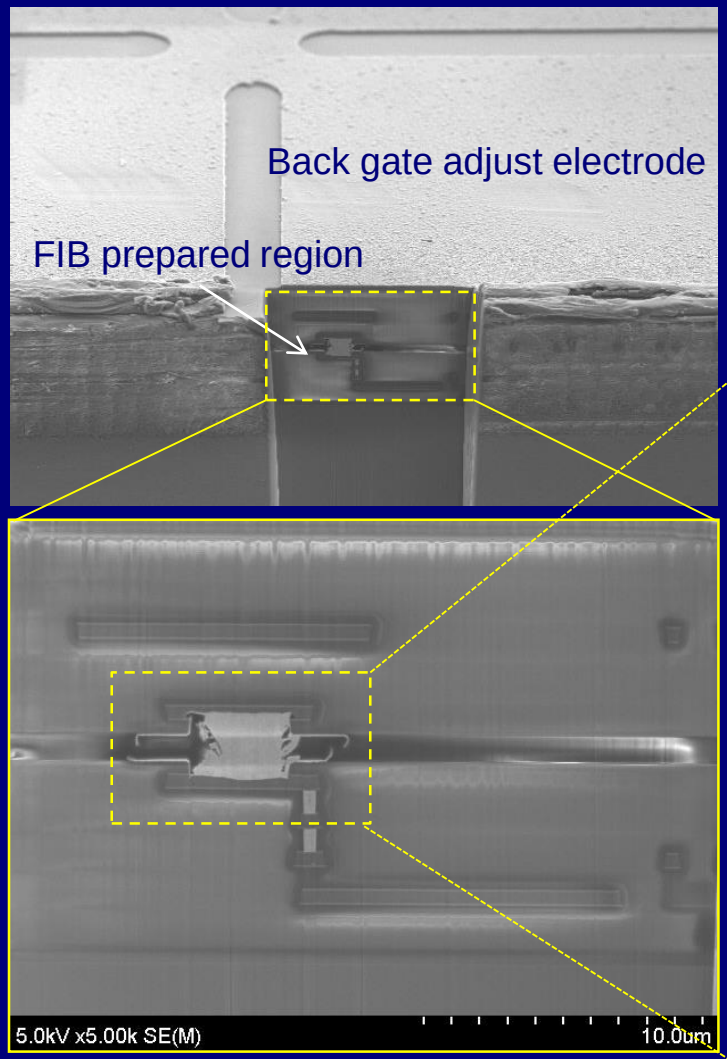
(d) Bulk-Si removal



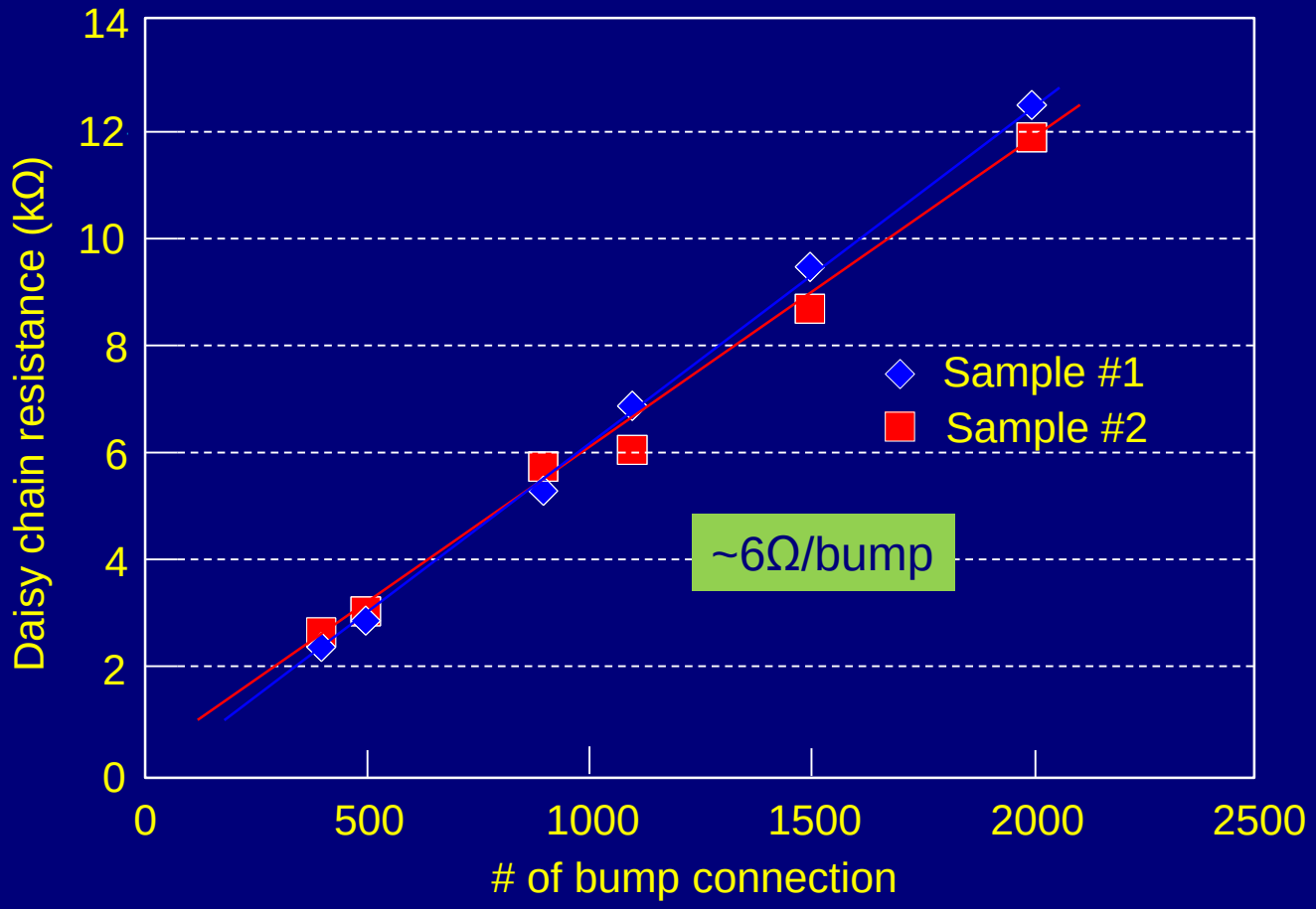
(e) Pad patterning and passivation



Cross section of Au cone bump junction



Daisy Chain Resistance

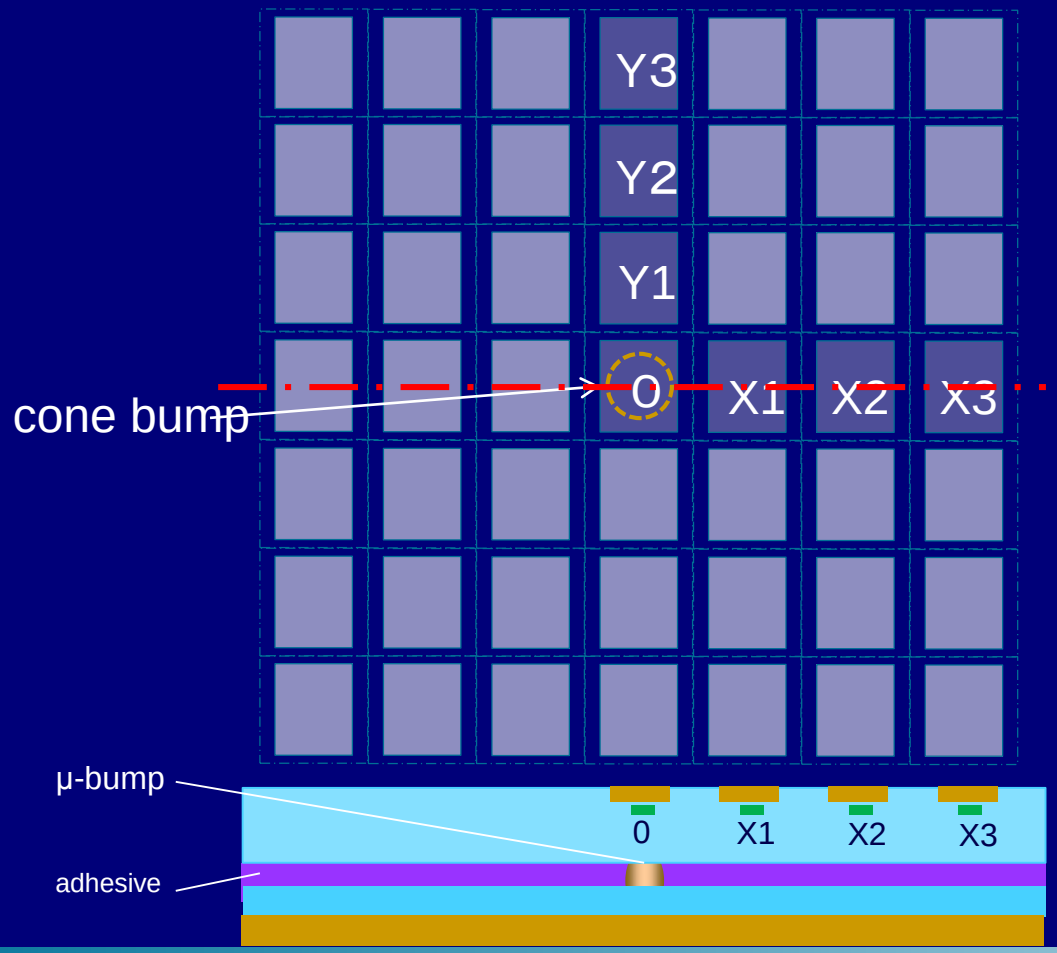


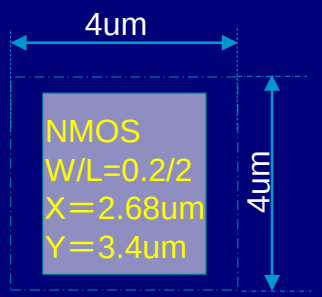
Ref. ～5Ω by 4 terminal resistance

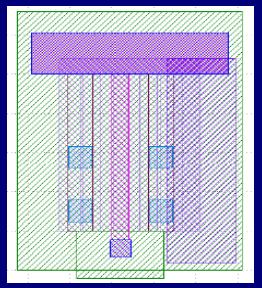
Stress evaluation

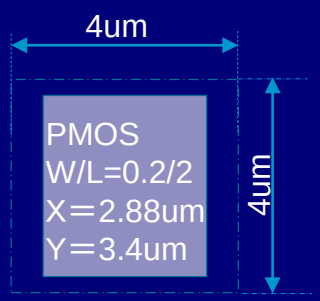
Evaluate the fluctuation of MOS Transistor caused by the stress of bump bonding

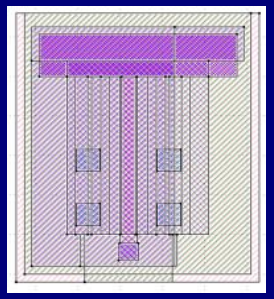
Device dimension N/P MOS Transistor W/L=2/0.2um











MOST I_{DS} vs V_{DS} Characteristics