Stacked SOI Pixel Detector using Versatile Fine Pitch μ-Bump Technology

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Abstract— **This Paper presents on 3D stacking technology with 2.5μm x 2.5μm In (Indium) bump connections with adhesive injection [1]. Instead of using the simple test device, this technology has been verified using the actual circuit level test chip. And it was found that the completion of stacking process is affected by the layout pattern of stacked each tier. In order to minimize those effects, we have optimized the layout, process parameter and device structure.**

I. Introduction

LSI technology has been widely spread in two dimensional over the past three decades and now, it moves into the era of sub-20nm node. In order to keep up the scaling trend, new transistors with 3D structure, new materials and processes have been introduced it. From economical view point, the development and manufacturing cost for SOC (System on Chip) has become sky-rocketing. The 3D-LSI is the one solution to suppress the increasing cost without degradation of performances [2]. By separating 3D-LSI technology into elementary technologies such as (1) through silicon via (TSV) formation, (2) bump formation, (3) wafer thinning, (4) chip/wafer alignment, and (5) chip/wafer bonding, many methods to realize 3D-LSI devices can be developed. We have been studying the 3D integration with μ-TSV and μ-bump with few μm dimension using simple test device and confirm the basic properties and reliability. In this paper, we focused on applying this technology to real circuit test device, SOI pixel detectors [3]. The simplest structure of 3D-pixel detectors are the two-tile face-to -face stacking devices with fine pitch μ-bump bonding, which requires bump formation, wafer thinning, chip/wafer alignment with small alignment error, and chip/wafer stacking techniques. As for bump connection, several methods were reported, such as Cu-Cu bonding, intermetallic-compound bonding with Cu/Sn bump, Au bump bonding, etc.[4],[5],[6],[7],[8]. The Cu-Cu direct bonding can provide good and robust connection, but it needs completely clean and surface flatness. Putting wafer/ chip stacking with bump bonding process into the actual production, it is difficult to make particle free environment. We think there must be a sort of redundancy in process in order to get high yield in mass production especially μ-bump with few μm dimension. So we have chosen the bump bonding with soft metal, such as In, and adhesive injection. One more merit of this structure is relaxing bonding stress. The highest process temperature is less than 200°C and pairs of opposite bumps are melted completely and make the robust electrical connections.

II. Pixel Detector

Pixel detector at collider is designed to collect information on particles come from the points where particles collide. Differ from the image sensors for digital camera, this device needs to detect fewer and much higher energy particles which pass through. The required key features of a pixel detector are high sensitivity and high signal processing speed. Fig.1 illustrates the schematic birds-view of silicon base SOI pixel detector [3]. SOI device provides both a high sensitivity

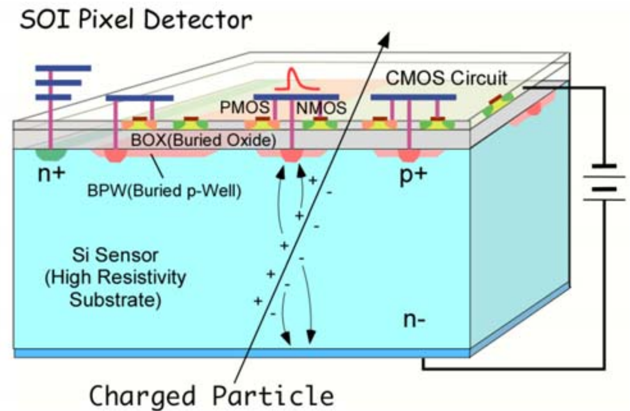

Fig.1 SOI pixel detector

sensor area in high resistivity bulk substrate and a high speed RO (readout) circuit area in SOI. Incident charged particle generates a bunch of hole-electron pairs along the trajectory in Si sensor and does not stop at all. The generated holes are collected by p+ diffusion layer in high resistivity Si substrate and sensed by the readout electronics circuits in SOI layer.

As the performance improvement, 3D integration is expected to increase space and time resolution, functionality without increase of pixel size. And 3D structure solves the back-gate effect for high voltage SOI device completely. For example, Sensors and analog circuits are fabricated in lower tier and digital circuits and I/Os are in upper tier.

III. PROCESS

Fig. 2 illustrates the process flow for SOI-3D chip stacking.

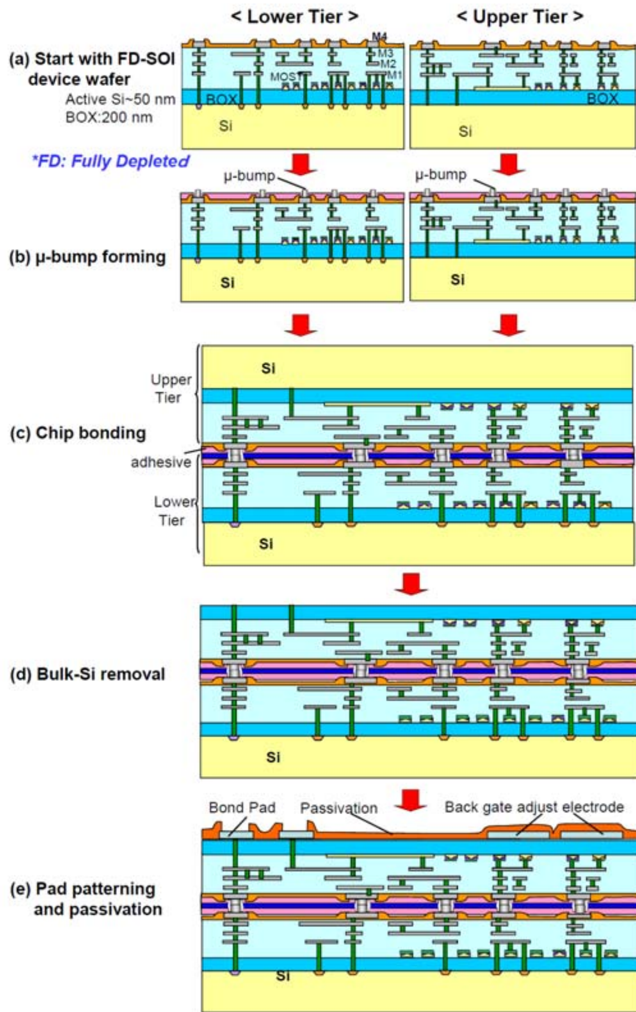

Fig. 2 Process flow for stacked SOI Pixel Detector

Base SOI chips as upper and lower tiers are fabricated using 8" ϕ 0.20um FD (Fully Depleted)-SOI process. Minimum bump pad opening size is 3μm x 3μm. Thickness of BOX (buried oxide) layer and SOI layer are 200nm and 40nm, respectively. After forming UBM, In bumps are formed using evaporation and lift-off technique. The minimum bump size and pitch are 2.5μm sq. and 5μm, respectively. Lower tier and upper tier are aligned using IR microscope. Initial alignment error before welding bumps must be kept less than 1.0μm in order to obtain stable electrical connection. After fusing into one connection, the tiers are self-aligned to below less than 0.6μm. The gap between tiers is about 1.5μm. An array of In μ-bump junctions does not have enough mechanical strength. So combining gap fill with adhesive is indispensable and injection method is the key of this process. Fig.3 shows the pixel detector chip before bonding and after bulk-silicon of upper tier removal.

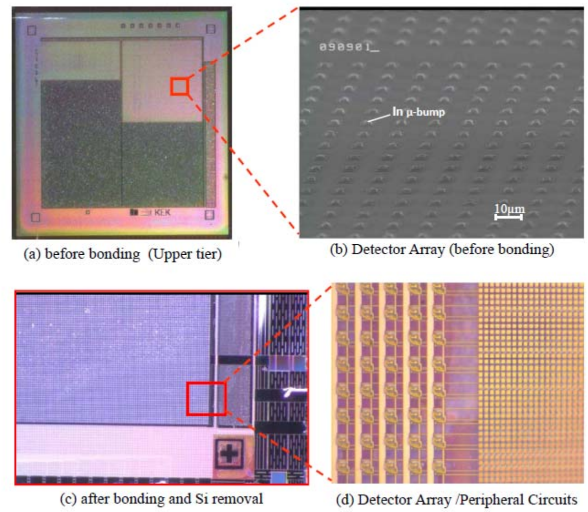

Fig. 3 Pixel detector chip before bonding and after Si removal

To avoid the agglomeration of small volume of In bumps, substrate must be keep low temperature during evaporation. After silicon removal, CMOS circuits and interconnects of lower tier can be observed by optical microscope through thin upper tier. We have been developing adhesive injection process using test wafers and test chips with relatively simple test pattern. But differ from using simple test chip, the space between tiers in an actual circuit test chip, which must be filled with adhesive is not uniform on entire chip. Checking the layout pattern where voids have been observed, the particular points of voids formation is found to be occur at the points where rapid pressure loss occurs (Fig.4) and near the adhesive flow passes which wrap around spaces.

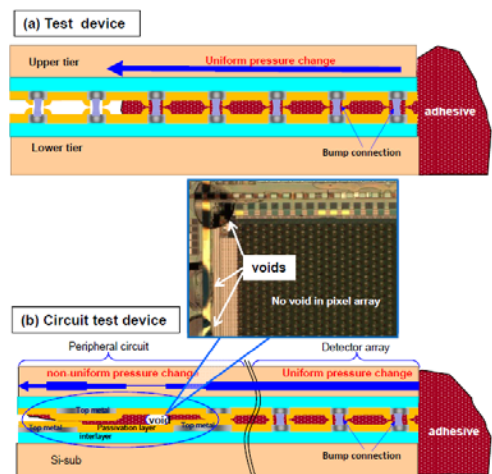

Fig. 4 Void formation Mechanism

Based on this mechanism, by optimizing bump and bump pad layout, process parameters with combining new injection method, such as controlled differential pressure assisted capillary action, the voids formation was completely suppressed, as shown in Fig.5.

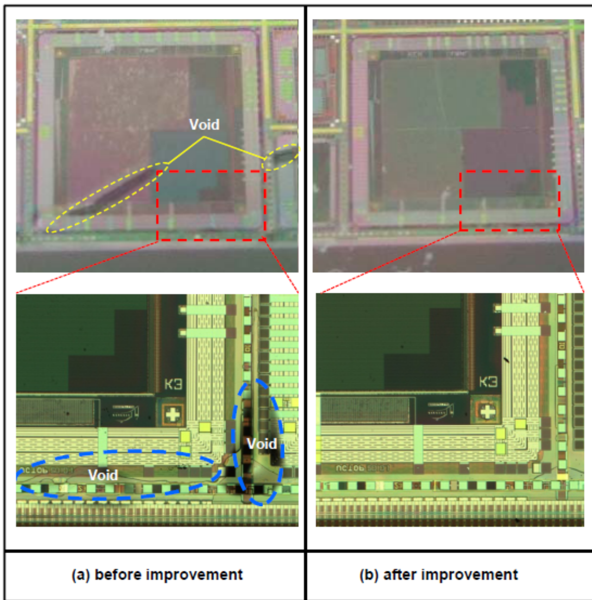

Fig.5 Result of counter measurement of void formation

It is also note about chip alignment, stacked tiers move slightly during adhesive curing. This occurs because the viscosity of adhesive decrease and In μ-bump became soft simultaneously in the early stage of curing. Reconsidering temperature profile of curing, alignment error could be minimized. Fig. 6 shows the bonding alignment marks at chip corner before and after improvement.

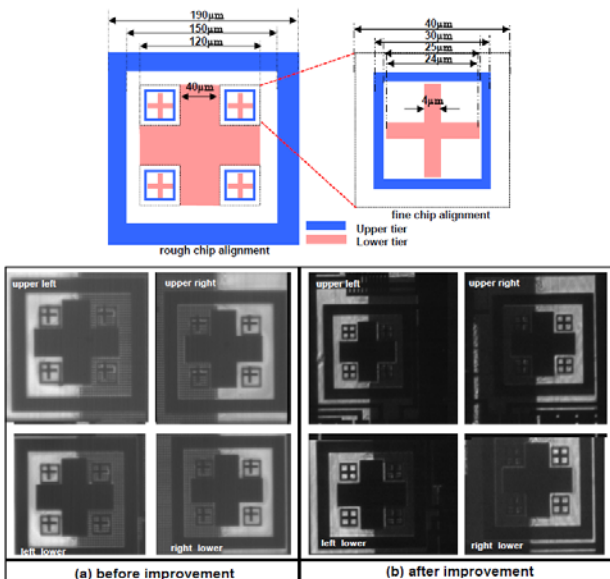

Fig. 6 Chip alignment after adhesive curing

Fig.7 shows the two types of pixel detectors. B pattern has large TEG area and therefore it has larger dispersion of M4 line projection density than that of A pattern. So in adhesive injection, careful process adjustment was needed. After silicon of upper tier removal, we checked the chip surface by optical microscope and found no void. The surface of both detector chips is covered by bond pads and back gate metal electrodes.

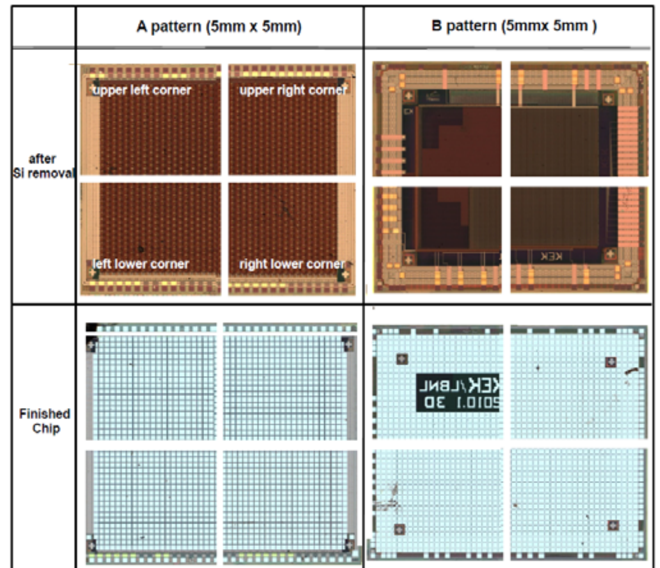

Fig. 7 Two type of pixel detector, (a) after Si removal,
(b) after finishing process

Fig. 8 shows SEM cross sectional image of pixel array. Thickness of upper tier is about 7μm. Top metal layer acts as back gate for FD-SOI MOS transistors in upper tier. If the bump pitch need to shrink to less than 5μm, it might be necessary to optimize the gap between tiers and volume of bump metal.

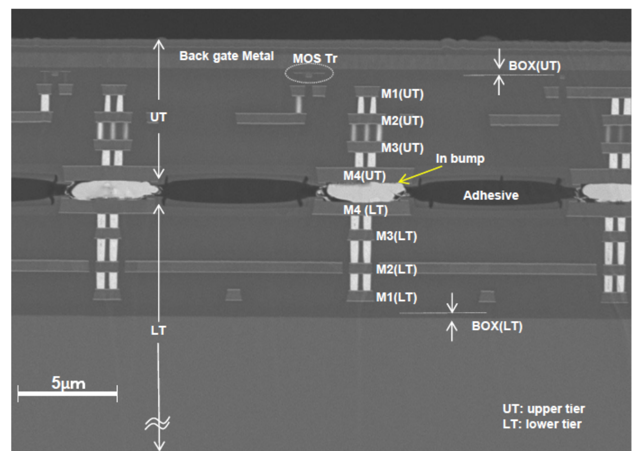

Fig. 8 Cross sectional SEM image of pixel array

IV. ELECTRICAL MEASUREMENT

In this device, there is new structure, bond pad connections with W-plug which we had not developed. Through interlayer and BOX via is formed during wafer process. W is exposed Si etchant and damaged. To checking this structure, the resistance between bond pads with same potential (eg. GND pads or VDD pads etc.) are evaluated. Although the measured resistance include resistances of vias and M1-M4 interconnect, these parasitic resistance are sufficient-low to judge good or not about the bond pad connection. Fig. 9 shows the result before and after cleaning.

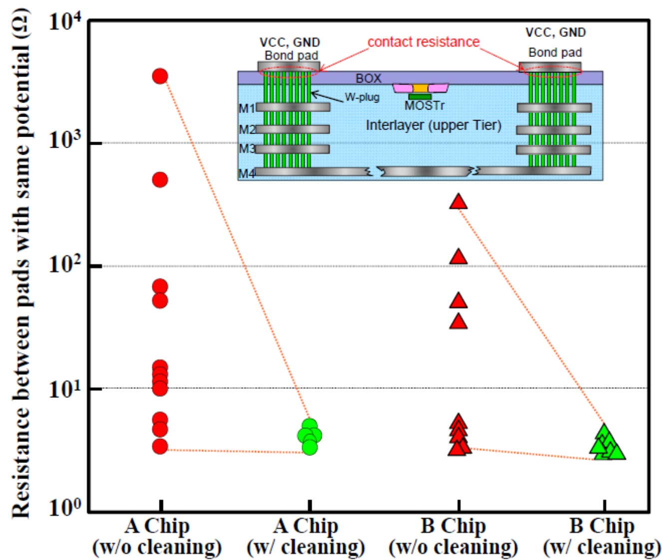

Fig. 9 Dispersion of Resistance between Bond Pads

As for μ-bump junction, the average bump resistance obtained for 2000 stages bump chain is about 30mΩ. This value closes to theoretical value calculated from the resistivity of In.

V. CONCLUSION

3D LSI Integration technology using minimum 5μm pitch bump is verified using SOI stacked pixel detector as circuit level test device. In this technology, adhesive injection is found the key technology. Optimizing layout, process parameter and adhesive injection method, this process have completed without void. If the bump pitch need to shrink to less than 5μm, it might be necessary to optimize the gap between tiers and volume of bump metal.

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