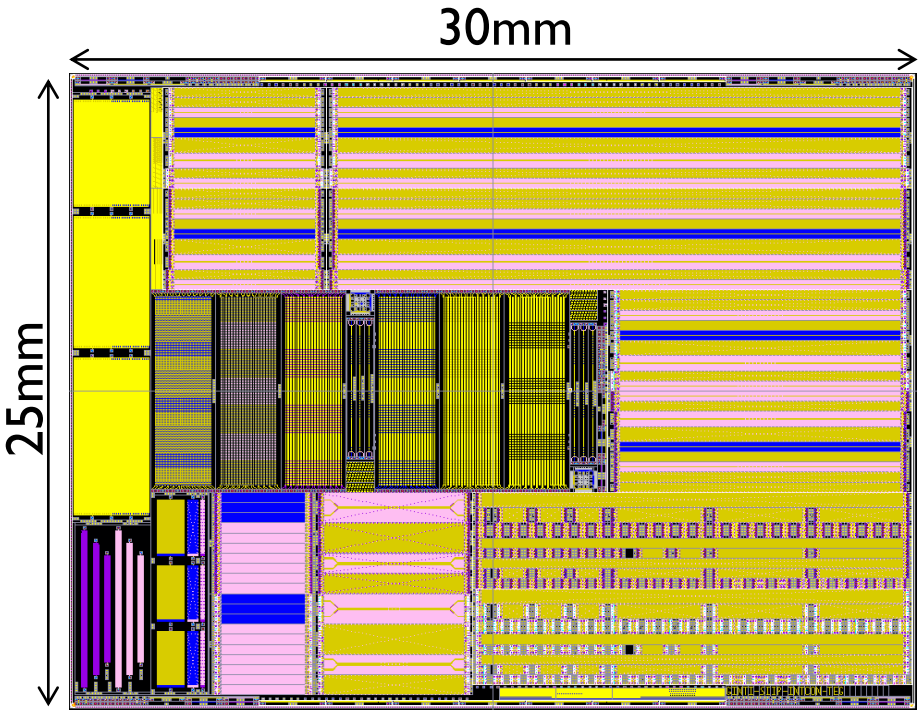
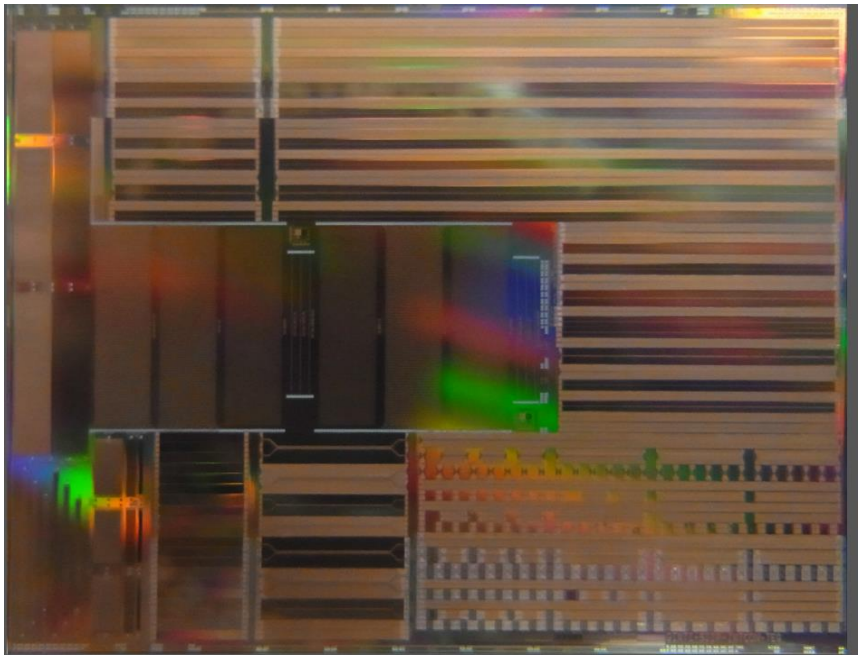
Si Interposer TEG Chip Layout and Chip Photo



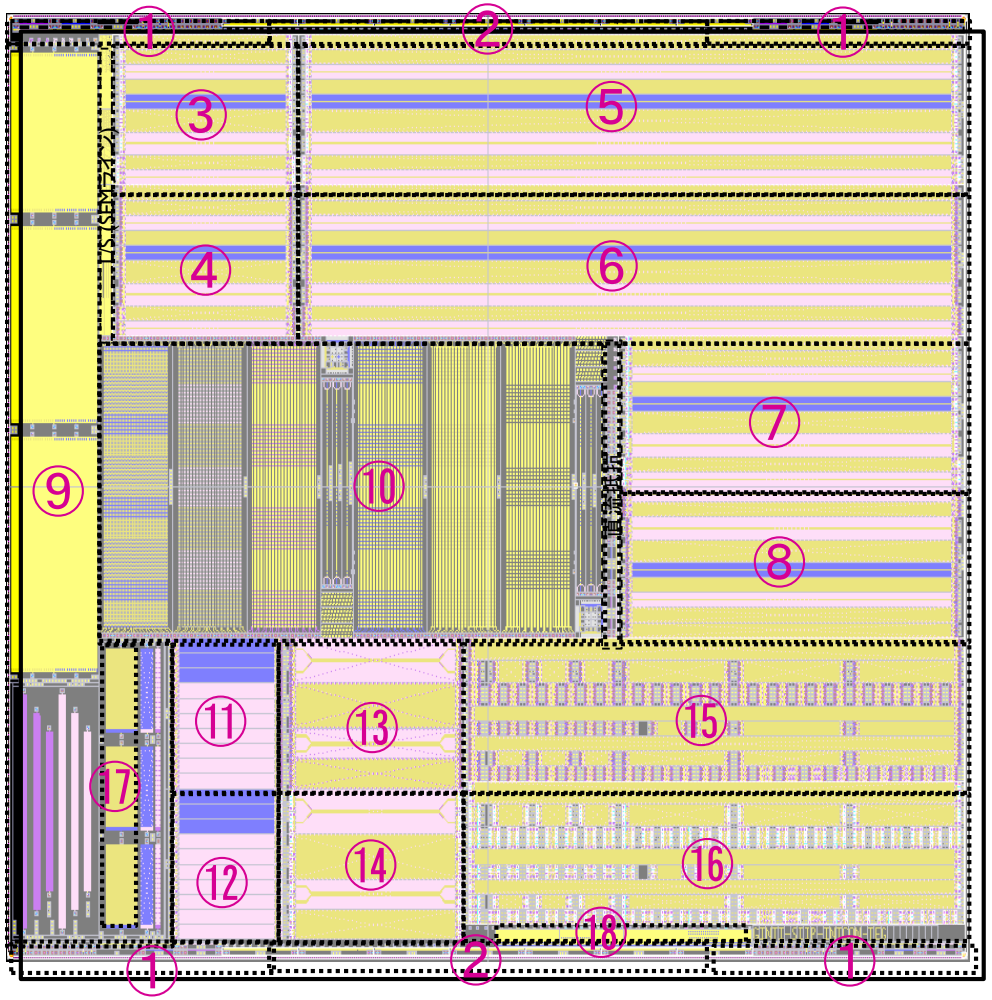
Layout



Chip photo

IM1
IV1 (via 1)
IM2
IV2
IM3
IV3
IM4
IV4
IM5 (Al pad (F))
Pad open
(UBM (F))
(Bump (F))
TSV
BRDL1
BPA
BRDL1 (Al pad (B))
Backside pad open
(UBM (B))
(Bump (B))

Evaluation Items in Si Interposer TEG Chip



①DC wiring resistance
②TSV electromigration
③Transmission line (5mm) (Front pad)
④Transmission line (5mm) (Backside pad)
⑤Transmission line (20mm) (Front pad)
⑥Transmission line (20mm) (Backside pad)
⑦Transmission line (10mm) (Front pad)
⑧Transmission line (10mm) (Backside pad)
⑨Capacitance
⑩Daisy chain
⑪Fine wiring (Backside)
⑫Fine wiring (Front)
⑬Cross talk (Backside pad)
⑭Cross talk (Front pad)
⑮Transmission line pad calibration (Backside pad)
⑯Transmission line pad calibration (Front pad)
⑰SEM pattern
⑱L/S (SEM pattern)